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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,147	03/06/2002	Shinichiro Tago	1614.1222	5917

21171	7590	07/28/2004	

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EXAMINER
GERSTL, SHANE F

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/091,147	TAGO ET AL.
	Examiner	Art Unit
	Shane F Gerstl	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *06 March 2002*.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-11* is/are pending in the application.
     4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) *1-11* is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on *06 March 2002* is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
     a) ☒ All   b) ☐ Some * c) ☐ None of:
       1. ☒ Certified copies of the priority documents have been received.
       2. ☐ Certified copies of the priority documents have been received in Application No. _____.
       3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
         application from the International Bureau (PCT Rule 17.2(a)).
     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
     Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-11 have been examined.

Papers Received

2.   Receipt is acknowledged of application papers submitted, where the papers have

been placed of record in the file.

Drawings

3.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4)

because reference character "S2" has been used to designate both a "No-Branching

Prediction" functional block in figure 3 and a "Register Address in BTB, and Store

Branch Outcome in Bias Bit" functional block in figure 4. Also, reference character "S3"

has been used to designate both a "PHT Hit?" decision block in figure 3 and an "Update

Address in BTB" functional block in figure 4, reference character "S4" has been used to

designate both a "Use Bias of BTB" functional block in figure 3 and a "PHT Hit?"

decision block in figure 4, and reference character "S5" has been used to designate

both a "Use Count Value of PHT" decision block in figure 3 and a "Prediction Correct?"

decision block in figure 4. Corrected drawing sheets are required in reply to the Office

action to avoid abandonment of the application. Any amended replacement drawing

sheet should include all of the figures appearing on the immediate prior version of the

sheet, even if only one figure is being amended. The replacement sheet(s) should be

labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to

obstruct any portion of the drawing figures. If the changes are not accepted by the

examiner, the applicant will be notified and informed of any required corrective action in

the next Office action. The objection to the drawings will not be held in abeyance.

4.   Figure 1 should be designated by a legend such as --Prior Art-- because only

that which is old is illustrated. The background section of the specification has

disclosed the description of figure 1 and that it is related art. Since this related art is

background material it is prior art. See MPEP § 608.02(g). Corrected drawing sheets

are required in reply to the Office action to avoid abandonment of the application. The

replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as

per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the

changes are not accepted by the examiner, the applicant will be notified and informed of

any required corrective action in the next Office action. The objection to the drawings

will not be held in abeyance.

Specification

5.   The title of the invention is not descriptive. A new title is required that is clearly

indicative of the invention to which the claims are directed.

The following title is suggested: Apparatus and Method for Branch Prediction

Where Data for Predictions is Selected from a Count in a Branch History Table or a Bias

in a Branch Target Buffer.

Claim Objections

6.   Claims 1, 6, 7, and 11 are objected to because of the following informalities: the

term "likelihood of branching" is unclear. This can be interpreted as the likelihood a

branch instruction will be encountered and executed or the likelihood that an executed

branch will be taken. The examiner is taking the claims to mean the likelihood that the branch will be taken based on the specification.

7.   Claim 3 is objected to because of the following informalities: the term "predicts no branching" is unclear. This can be interpreted as predicting a branch instruction will not be encountered and executed or predicting that an executed branch will be not taken. The examiner is taking the claims to mean predicting that the branch will not be taken based on the specification.

8.   Claim 7 is objected to because of the following informalities: the word "previous" is misspelled in line 33.

Appropriate correction is required

Claim Rejections - 35 USC § 103

9.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10.   Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henry (6,550,004) in view of Shiell (6,108,775).

11.   In regard to claim 1,

        a.   Henry has disclosed an apparatus for branch prediction, comprising:

                i.   a history register (figures 2 and 3, element 216) which stores therein history of previous branch instructions;

ii.   an index generation circuit which generates a first index from an instruction address and the history stored in said history register (figure 3, element 312);

iii.   a history table (figure 3, element 302) which stores therein a portion of the instruction address as a tag and a first value indicative of likelihood of branching in association with the first index; [Column 8, lines 31-40 show that the history table is indexed by a hash value equal to a modified portion of the address , or a tag. Lines 50-55 show that the table also holds an Agree/Disagree bit. Lines 21-30 show that this bit is used to make a branch prediction or determine the likelihood a branch is taken.]

iv.   a buffer indicated by the instruction address and a second value indicative of likelihood of branching in association with a second index that is at least a portion of the instruction address; Figures 2 and 3 and the sections cited above show that a second dynamic branch predictor (element 204) is used to indicate and store (thus a buffer) the likelihood of a branch being taken and is indexed by a function of a portion of the instruction address.

v.   and a selection unit which makes a branch prediction by selecting one of the first value and the second value (figure 2, element 206.)

b.   Henry has not disclosed the buffer being a branch destination buffer which stores therein a branch destination address or predicted branch destination address of an instruction;

c.   Shiell has disclosed the use of a dynamic branch predictor that is a branch destination buffer or branch target buffer that stores a branch destination or target address of an instruction and is indexed by tags (portion of the instruction address) as discussed in column 2, lines 12-34.

d.   Shiell has also shown in this section that this branch target buffer is more accurate than a predictor that keeps track of other branches (such as a plain history table) by keeping track of each branch's history. In addition, by storing the target address, the destination may be fetched immediately based on the prediction without calculating the instruction address and thus instruction fetching is quicker. The ability to have more accurate branch prediction and speed up instruction fetching would have motivated one of ordinary skill in the art to modify the design of Henry to use the branch destination buffer taught by Shiell as the dynamic branch predictor (element 204) of Henry.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Henry to use the branch destination buffer of Shiell as the dynamic branch predictor 204 of Henry so that more accurate prediction is used and instruction fetching is sped up.

12.   In regard to claim 2, Henry in view of Shiell discloses the apparatus as claimed in claim 1, wherein

a.   said selection unit selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address

and current history; [Figure 5, case 1 shows that the X predictor (history table) is selected (selector agrees (A) with the static prediction X) when both X and Y (BTB) are correct and thus they both must have a corresponding value.]

b.   and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history. [Figure 5, case 11 shows that the X (table) predictor was wrong and the Y (BTB) predictor was correct. Thus the Y predictor had a corresponding entry and the X predictor either had a wrong value or did not have an entry both of which give a wrong prediction. In this case the BTB was selected.]

13.   In regard to claim 3, Henry in view of Shiell discloses the apparatus as claimed in claim 2, wherein said selection unit predicts no branching if said branch destination buffer does not have an entry therein corresponding to the current instruction address. [Figure 5, cases 13-16 of Henry illustrates when both predictors are wrong, which includes the case where neither have a corresponding entry. Here the static prediction is either agreed or disagreed with and as shown throughout the disclosure the prediction is either "taken" or "not taken" and thus there are instances where the prediction is not taken.

14.   In regard to claim 4, Henry in view of Shiell discloses the apparatus as claimed in claim 1, wherein said index generation circuit generates the first index that is an

Exclusive-OR between the history stored in said history register and the current

instruction address (figure 3).

15.   In regard to claim 5,

    a.   Henry in view of Shiell discloses the apparatus as claimed in claim 1.

    b.   Henry in view of Shiell does not disclose wherein more than one said

history table is provided so as to allow a plurality of entries to be registered with

respect to said first index.

    c.   While a plurality of history tables is not explicitly taught, a single history

table is taught as shown above. The inclusion of a plurality of history tables to

perform the same claimed function as a single history table provides no new or

unexpected result over the prior art. Therefore, one of ordinary skill in the art

would have found it obvious to duplicate the fetch module, creating a fetch

module for each pipeline. With multiple duplicate history tables in place, multiple

entries in the multiple tables would inherently be allowed to be register with the

same index since each table is a duplicate (see MPEP 2144.04 (VI): In re Harza,

274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

16.   In regard to claim 6,

    a.   Henry in view of Shiell discloses a processor (figure 1), comprising:

        i.   a history register (figures 2 and 3, element 216) which stores

        therein history of previous branch instructions;

ii.   an index generation circuit (figure 3, element 312) which generates

a first index from an instruction address and the history stored in said

history register;

iii.   a history table (figure 3, element 302) which stores therein a portion

of the instruction address as a tag and a first value indicative of likelihood

of branching in association with the first index; [Column 8, lines 31-40

show that the history table is indexed by a hash value equal to a modified

portion of the address , or a tag. Lines 50-55 show that the table also

holds an Agree/Disagree bit. Lines 21-30 show that this bit is used to

make a branch prediction or determine the likelihood a branch is taken.]

iv.   a buffer indicated by the instruction address and a second value

indicative of likelihood of branching in association with a second index that

is at least a portion of the instruction address; Figures 2 and 3 and the

sections cited above show that a second dynamic branch predictor

(element 204) is used to indicate and store (thus a buffer) the likelihood of

a branch being taken and is indexed by a function of a portion of the

instruction address.

v.   a selection unit which makes a branch prediction by selecting one

of the first value and the second value (figure 2, element 206);

vi.   an execution control unit which controls execution of instructions

and an execution operation unit (figure 1, element 109) which executes

the instructions. [The execution unit inherently has control logic to control it.]

b.   Henry has not disclosed the buffer being a branch destination buffer which stores therein a branch destination address or predicted branch destination address of an instruction;

c.   Shiell has disclosed the use of a dynamic branch predictor that is a branch destination buffer or branch target buffer that stores a branch destination or target address of an instruction and is indexed by tags (portion of the instruction address) as discussed in column 2, lines 12-34.

d.   Shiell has also shown in this section that this branch target buffer is more accurate than a predictor that keeps track of other branches (such as a plain history table) by keeping track of each branch's history. In addition, by storing the target address, the destination may be fetched immediately based on the prediction without calculating the instruction address and thus instruction fetching is quicker. The ability to have more accurate branch prediction and speed up instruction fetching would have motivated one of ordinary skill in the art to modify the design of Henry to use the branch destination buffer taught by Shiell as the dynamic branch predictor (element 204) of Henry.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Henry to use the branch destination buffer of Shiell as the dynamic branch predictor 204 of Henry so that more accurate prediction is used and instruction fetching is sped up.

17.   In regard to claim 7,

a.   Henry in view of Shiell discloses a method of branch prediction,

comprising the steps of:

i.   providing a history table (figure 3, element 302) which stores

therein a portion of an instruction address as a tag and a first value

indicative of likelihood of branching in association with a first index that is

generated from the instruction address and history of previous branch

instructions; [Column 8, lines 31-40 show that the history table is indexed

by a hash value equal to a modified portion of the address , or a tag.

Lines 50-55 show that the table also holds an Agree/Disagree bit. Lines

21-30 show that this bit is used to make a branch prediction or determine

the likelihood a branch is taken.]

ii.   providing a buffer (interpreted as hardware as indicate in the

specification in order to avoid 35 USC 101 problems) indicated by the

instruction address and a second value indicative of likelihood of

branching in association with a second index that is at least a portion of

the instruction address; Figures 2 and 3 and the sections cited above

show that a second dynamic branch predictor (element 204) is used to

indicate and store (thus a buffer) the likelihood of a branch being taken

and is indexed by a function of a portion of the instruction address.

iii.   selecting one of a first value and a second value (using figure 2,

element 206);

iv. and predicting branching in response to the selected one of the first value and the second value (figure 2, element 189 gives T for taken or NT for not taken).

b. Henry has not disclosed the buffer being a branch destination buffer which stores therein a branch destination address or predicted branch destination address of an instruction;

c. Shiell has disclosed the use of a dynamic branch predictor that is a branch destination buffer or branch target buffer that stores a branch destination or target address of an instruction and is indexed by tags (portion of the instruction address) as discussed in column 2, lines 12-34.

d. Shiell has also shown in this section that this branch target buffer is more accurate than a predictor that keeps track of other branches (such as a plain history table) by keeping track of each branch's history. In addition, by storing the target address, the destination may be fetched immediately based on the prediction without calculating the instruction address and thus instruction fetching is quicker. The ability to have more accurate branch prediction and speed up instruction fetching would have motivated one of ordinary skill in the art to modify the design of Henry to use the branch destination buffer taught by Shiell as the dynamic branch predictor (element 204) of Henry.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Henry to use the branch destination buffer of Shiell as the dynamic

branch predictor 204 of Henry so that more accurate prediction is used and instruction

fetching is sped up.

18.   In regard to claim 8, Henry in view of Shiell discloses the method as claimed in

claim 7, wherein

> a.   said step of selecting one of the first value and the second value selects
>
> the first value if said branch destination buffer has an entry therein corresponding
>
> to a current instruction address and said history table has an entry therein
>
> corresponding to the current instruction address and current history; [Figure 5,
>
> case 1 shows that the X predictor (history table) is selected (selector agrees (A)
>
> with the static prediction X) when both X and Y (BTB) are correct and thus they
>
> both must have a corresponding value.]
>
> b.   and selects the second value if said branch destination buffer has an entry
>
> therein corresponding to the current instruction address and said history table
>
> does not have an entry therein corresponding to the current instruction address
>
> and the current history. [Figure 5, case 11 shows that the X (table) predictor was
>
> wrong and the Y (BTB) predictor was correct. Thus the Y predictor had a
>
> corresponding entry and the X predictor either had a wrong value or did not have
>
> an entry both of which give a wrong prediction. In this case the BTB was
>
> selected.]

19.   In regard to claim 9, Henry in view of Shiell discloses the method as claimed in

claim 8, further comprising the steps of:

a.   registering the current instruction address in said branch destination buffer

if said branch destination buffer does not have an entry therein corresponding to

the current instruction address (Shiell, column 2, lines 28-34);

b.   and registering information about the current instruction address in the

history table if said branch destination buffer has an entry therein corresponding

to the current instruction address and said history table does not have an entry

therein corresponding to the current instruction address and the current history

and if a prediction made based on the second value turns out to be erroneous.

[This above cited section also shows that current entries are modified based on

the branch outcome, including times when there was an erroneous prediction.

This happens regardless of the other table, so the update occurs at time when

there is no entry in the history table.]

20.   In regard to claim 10, Henry in view of Shiell discloses the method as claimed in

claim 9, wherein the information about the current instruction address is not registered

in said history table if said branch destination buffer has an entry therein corresponding

to the current instruction address and said history table does not have an entry therein

corresponding to the current instruction address and the current history and if the

prediction made based on the second value turns out to be correct. [Figure 5 of Shiell

shows cases (10 and 11 for example) where the BTB (Y) prediction was correct and the

history table (X) was incorrect (which includes if it does not have an entry since it thus

cannot be correct) and where the history table (X) was not updated.]

21.   In regard to claim 11,

a.   Henry in view of Shiell discloses an apparatus for branch prediction,

comprising:

i.   a history register (figures 2 and 3, element 216) which stores

therein history of immediately preceding branch instructions;

ii.   an index generation circuit which generates a first index that is an

Exclusive-OR between an instruction address and the history stored in

said history register (figure 3, element 312);

iii.   a history table (figure 3, element 302) which stores therein a portion

of the instruction address as a tag and a first value indicative of likelihood

of branching in association with each said first index; [Column 8, lines 31-

40 show that the history table is indexed by a hash value equal to a

modified portion of the address , or a tag. Lines 50-55 show that the table

also holds an Agree/Disagree bit. Lines 21-30 show that this bit is used to

make a branch prediction or determine the likelihood a branch is taken.]

iv.   a buffer indicated by the instruction address and a second value

indicative of likelihood of branching in association with a second index that

is at least a portion of the instruction address; Figures 2 and 3 and the

sections cited above show that a second dynamic branch predictor

(element 204) is used to indicate and store (thus a buffer) the likelihood of

a branch being taken and is indexed by a function of a portion of the

instruction address;

v.   and a selection unit (figure 2, element 206) which makes a branch

prediction by selecting one of the first value and the second value,

wherein said selection unit selects the first value if said branch destination

buffer has an entry therein corresponding to a current instruction address

and said history table has an entry therein corresponding to the current

instruction address and current history, and selects the second value if

said branch destination buffer has an entry therein corresponding to the

current instruction address and said history table does not have an entry

therein corresponding to the current instruction address and the current

history. [Figure 5, case 1 shows that the X predictor (history table) is

selected (selector agrees (A) with the static prediction X) when both X and

Y (BTB) are correct and thus they both must have a corresponding value.

Figure 5, case 11 shows that the X (table) predictor was wrong and the Y

(BTB) predictor was correct. Thus the Y predictor had a corresponding

entry and the X predictor either had a wrong value or did not have an entry

both of which give a wrong prediction. In this case the BTB was selected.]

b.   Henry has not disclosed the buffer being a branch destination buffer which

stores therein a branch destination address or predicted branch destination

address of an instruction;

c.   Shiell has disclosed the use of a dynamic branch predictor that is a branch

destination buffer or branch target buffer that stores a branch destination or

target address of an instruction and is indexed by tags (portion of the instruction address) as discussed in column 2, lines 12-34.

d.   Shiell has also shown in this section that this branch target buffer is more accurate than a predictor that keeps track of other branches (such as a plain history table) by keeping track of each branch's history. In addition, by storing the target address, the destination may be fetched immediately based on the prediction without calculating the instruction address and thus instruction fetching is quicker. The ability to have more accurate branch prediction and speed up instruction fetching would have motivated one of ordinary skill in the art to modify the design of Henry to use the branch destination buffer taught by Shiell as the dynamic branch predictor (element 204) of Henry.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Henry to use the branch destination buffer of Shiell as the dynamic branch predictor 204 of Henry so that more accurate prediction is used and instruction fetching is sped up.

Conclusion

22.   The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

23.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. The following patents have been cited to further show the art with

respect to dynamic branch prediction in general.

US Pat No 6,516,409 to Sato teaches a dynamic branch predictor that indicates

taken or not taken and is indexed by an address tag.

US Pat No 5,864,697 to Shiell had disclosed the use of a BTB and pattern history

table for two-level prediction.

US Pat No 6,421,774 to Henry is incorporated by reference in the Henry citation

above and is pertinent.

US Pat No 6,247,122 to Henry is incorporated by reference in the Henry citation

above and is pertinent

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Shane F Gerstl whose telephone number is (703)305-

7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).
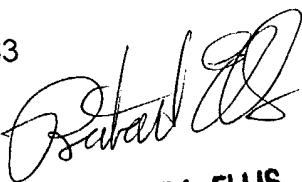
If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

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Shane F Gerstl
Examiner
Art Unit 2183

SFG
7/23/04

RICHARD L. ELLIS
PRIMARY EXAMINER